Abstract of the Disclosure

An effective structure of a pixel cache for use in a three-dimensional (3D) graphics accelerator is provided. The pixel cache includes a z-data storage unit that reads z-data from a frame memory and provides the read z-data to a pixel rasterization pipeline; and a color data storage unit that in advance reads and stores color data from the frame memory at the same time when the z-data storage unit reads the z-data from the frame memory, and provides the color data to the pixel rasterization pipeline only when the result of predetermined z-test is determined to be a success in the pixel rasterization pipeline. Accordingly, the pixel cache structure enables only color data required to be read and stored in advance before processing of the color data, thereby preventing access latency, increasing the efficiency of a color cache, and reducing power consumption.